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Semiconductor Electronics : Materials, Devices and Simple Circuits

TOPIC 1 Solids, Semiconductors and P-N Junction Diode

1. With increasing biasing voltage of a photodiode, the photocurrent magnitude : **[Sep. 05, 2020 (I)]**

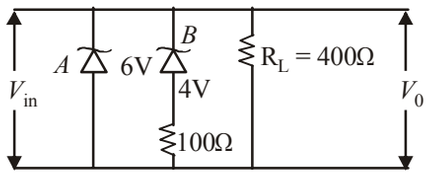
(a) remains constant

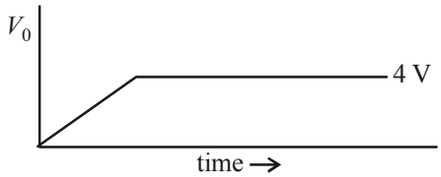
(b) increases initially and after attaining certain value, it decreases

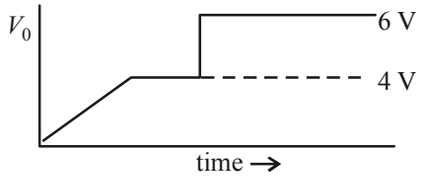
(c) Increases linearly

(d) increases initially and saturates finally

2. Two Zener diodes (A and B) having breakdown voltages of 6 V and 4 V respectively, are connected as shown in the circuit below. The output voltage V_0 variation with input voltage linearly increasing with time, is given by :
($V_{input} = 0$ V at $t = 0$)
(figures are qualitative) **[Sep. 05, 2020 (II)]**



(a)


(b)


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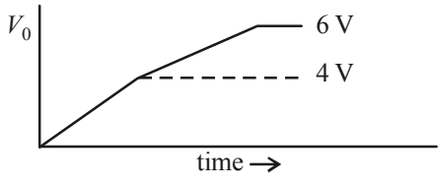

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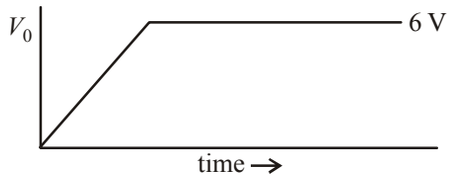
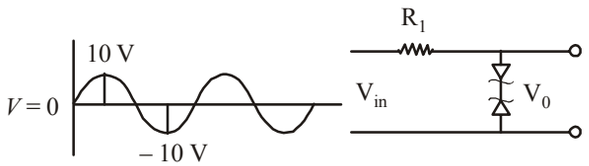
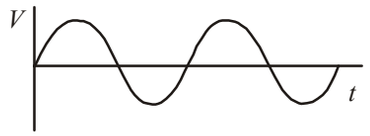
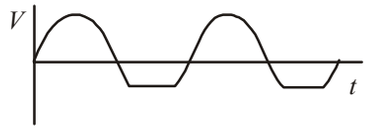


3. Take the breakdown voltage of the zener diode used in the given circuit as 6V. For the input voltage shown in figure below, the time variation of the output voltage is :
(Graphs drawn are schematic and not to scale)
[Sep. 04, 2020 (I)]



(a)


(b)


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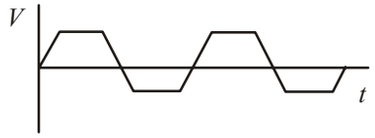
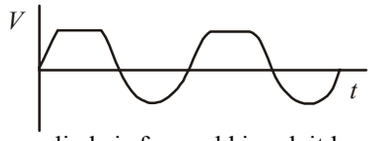


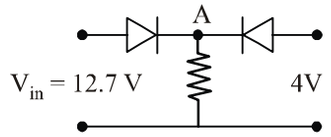
(d)


4. When a diode is forward biased, it has a voltage drop of 0.5 V. The safe limit of current through the diode is 10 mA. If a battery of emf 1.5 V is used in the circuit, the value of minimum resistance to be connected in series with the diode so that the current does not exceed the safe limit is : **[Sep. 03, 2020 (I)]**

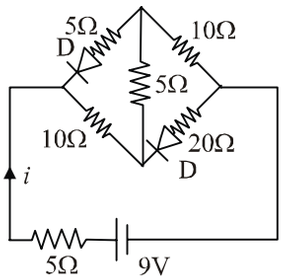
(a) 300 Ω (b) 50 Ω
(c) 100 Ω (d) 200 Ω

5. If a semiconductor photodiode can detect a photon with a maximum wavelength of 400 nm, then its band gap energy is:
Planck's constant, $h = 6.63 \times 10^{-34}$ J.s.
Speed of light, $c = 3 \times 10^8$ m/s **[Sep. 03, 2020 (II)]**
(a) 1.1 eV (b) 2.0 eV
(c) 1.5 eV (d) 3.1 eV

6. Both the diodes used in the circuit shown are assumed to be ideal and have negligible resistance when these are forward biased. Built in potential in each diode is 0.7 V. For the input voltages shown in the figure, the voltage (in Volts) at point A is _____. **[NA 9 Jan. 2020 I]**

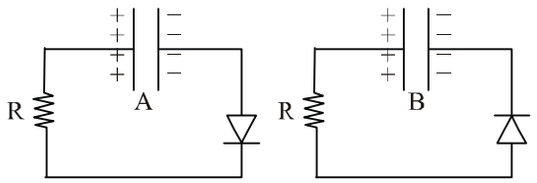


7. The current i in the network is: **[9 Jan. 2020 II]**



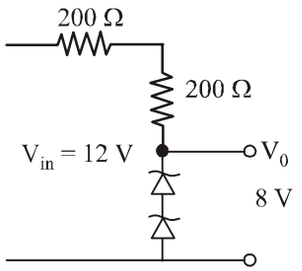
(a) 0.2 A (b) 0.6 A (c) 0.3 A (d) 0 A

8. Two identical capacitors A and B, charged to the same potential 5V are connected in two different circuits as shown below at time $t = 0$. If the charge on capacitors A and B at time $t = CR$ is Q_A and Q_B respectively, then (Here e is the base of natural logarithm) **[9 Jan. 2020 II]**

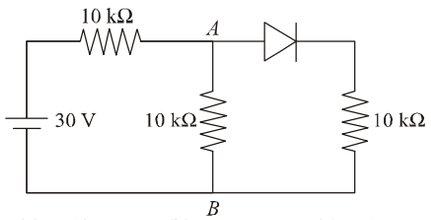


(a) $Q_A = \frac{VC}{e}, Q_B = \frac{CV}{2}$ (b) $Q_A = VC, Q_B = CV$
(c) $Q_A = VC, Q_B = \frac{VC}{e}$ (d) $Q_A = \frac{CV}{2}, Q_B = \frac{VC}{e}$

9. The circuit shown below is working as a 8 V dc regulated voltage source. When 12 V is used as input, the power dissipated (in mW) in each diode is; (considering both zener diodes are identical) _____. **[NA 9 Jan. 2020 II]**

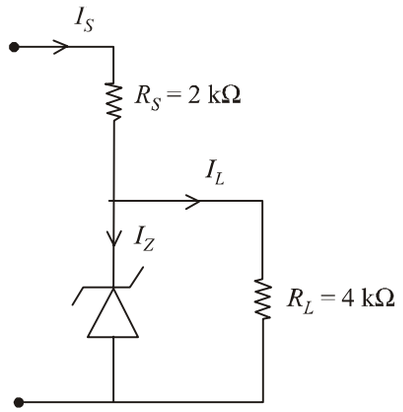


10. In the figure, potential difference between A and B is: **[7 Jan. 2020 II]**



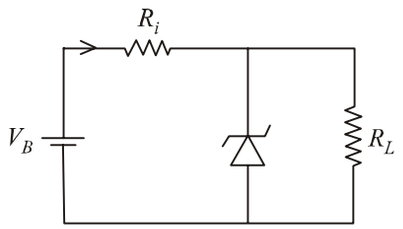
(a) 10 V (b) 5 V (c) 15 V (d) zero

11. Figure shows a DC voltage regulator circuit, with a Zener diode of breakdown voltage = 6V. If the unregulated input voltage varies between 10 V to 16 V, then what is the maximum Zener current ? **[12 Apr. 2019 II]**



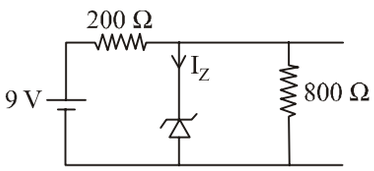
(a) 2.5 mA (b) 1.5 mA (c) 7.5 mA (d) 3.5 mA

12. The figure represents a voltage regulator circuit using a Zener diode. The breakdown voltage of the Zener diode is 6 V and the load resistance is $R_L = 4$ k. The series resistance of the circuit is R_i=1k. If the battery voltage V_B varies from 8 V to 16 V, what are the minimum and maximum values of the current through Zener diode ? **[10 Apr. 2019 II]**



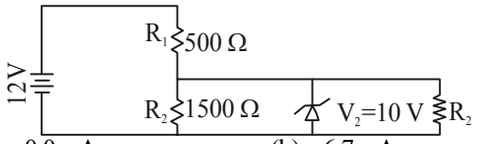
(a) 0.5 mA; 6 mA (b) 1 mA; 8.5 mA
(c) 0.5 mA; 8.5 mA (d) 1.5 mA; 8.5 mA

13. The reverse breakdown voltage of a Zener diode is 5.6 V in the given circuit.



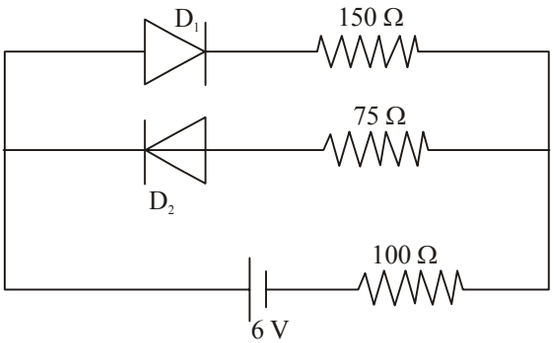
The current I_z through the Zener is : **[8 April 2019 I]**
(a) 10 mA (b) 17 mA
(c) 15 mA (d) 7 mA

14. In the given circuit the current through Zener Diode is close to : **[11 Jan. 2019 I]**



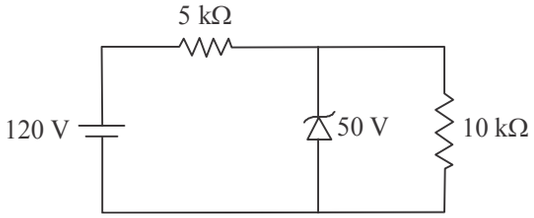
(a) 0.0 mA (b) 6.7 mA
(c) 4.0 mA (d) 6.0 mA

15. The circuit shown below contains two ideal diodes, each with a forward resistance of 50 Ω. If the battery voltage is 6V, the current through the 100 Ω resistance (in Amperes) is : **[11 Jan. 2019 II]**



(a) 0.036 (b) 0.020
(c) 0.027 (d) 0.030

16. For the circuit shown below, the current through the Zener diode is: **[10 Jan. 2019 II]**

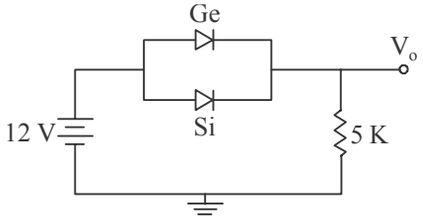


(a) 9 mA (b) 5 mA
(c) Zero (d) 14 mA

17. Mobility of electrons in a semiconductor is defined as the ratio of their drift velocity to the applied electric field. If, for an n-type semiconductor, the density of electrons is 10^{19} m^{-3} and their mobility is $1.6 m^2/(V.s)$ then the resistivity of the semiconductor (since it is an n-type semiconductor contribution of holes is ignored) is close to: **[9 Jan. 2019 I]**

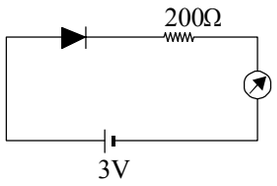
(a) 2 Ωm (b) 4 Ωm (c) 0.4 Ωm (d) 0.2 Ωm

18. Ge and Si diodes start conducting at 0.3 V and 0.7 V respectively. In the following figure if Ge diode connection are reversed, the value of V_o changes by : (assume that the Ge diode has large breakdown voltage) **[9 Jan. 2019 II]**



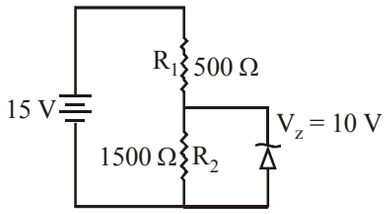
(a) 0.8 V (b) 0.6 V
(c) 0.2 V (d) 0.4 V

19. The reading of the ammeter for a silicon diode in the given circuit is : **[2018]**



(a) 0 (b) 15 mA
(c) 11.5 mA (d) 13.5 mA

20. In the given circuit, the current through zener diode is: **[Online April 16, 2018]**



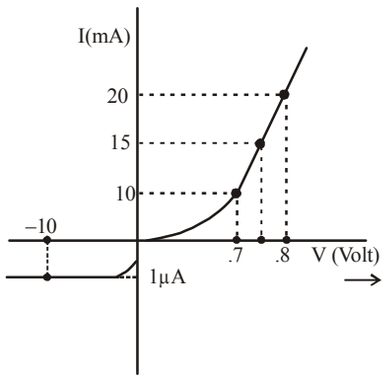
(a) 2.5mA (b) 3.3mA
(c) 5.5mA (d) 6.7mA

21. What is the conductivity of a semiconductor sample having electron concentration of 5×10^{18} m^{-3}, hole concentration of 5×10^{19} m^{-3}, electron mobility of 2.0 $m^2 V^{-1} s^{-1}$ and hole mobility of 0.01 $m^2 V^{-1} s^{-1}$? **[Online April 8, 2017]**

(Take charge of electron as 1.6×10^{-19} C)

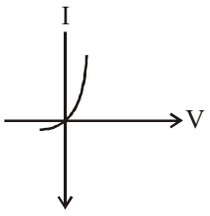
(a) $1.68\ (\Omega - m)^{-1}$ (b) $1.83\ (\Omega - m)^{-1}$
(c) $0.59\ (\Omega - m)^{-1}$ (d) $1.20\ (\Omega - m)^{-1}$

22. The V–I characteristic of a diode is shown in the figure. The ratio of forward to reverse bias resistance is : **[Online April 8, 2017]**

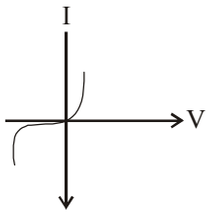


(a) 10 (b) 10^{-6}
(c) 10^6 (d) 100

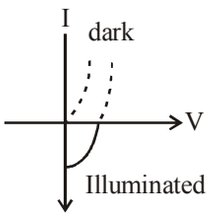
23. Identify the semiconductor devices whose characteristics are given below, in the order (i), (ii), (iii), (iv) : **[2016]**



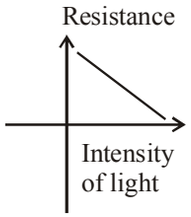
(i)



(ii)



(iii)



(iv)

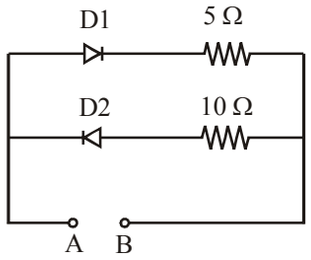
(a) Solar cell, Light dependent resistance, Zener diode, simple diode
(b) Zener diode, Solar cell, simple diode, Light dependent resistance
(c) Simple diode, Zener diode, Solar cell, Light dependent resistance
(d) Zener diode, Simple diode, Light dependent resistance, Solar cell

24. The temperature dependence of resistances of Cu and undoped Si in the temperature range 300-400 K, is best described by : **[2016]**
(a) Linear increase for Cu, exponential decrease of Si.
(b) Linear decrease for Cu, linear decrease for Si.
(c) Linear increase for Cu, linear increase for Si.
(d) Linear increase for Cu, exponential increase for Si.

25. An experiment is performed to determine the I–V characteristics of a Zener diode, which has a protective resistance of R = 100 Ω, and a maximum power of dissipation rating of 1W. The minimum voltage range of the DC source in the circuit is : **[Online April 9, 2016]**
(a) 0–5V (b) 0–24 V
(c) 0–12 V (d) 0–8V

26. A red LED emits light at 0.1 watt uniformly around it. The amplitude of the electric field of the light at a distance of 1 m from the diode is : **[2015]**
(a) 5.48 V/m (b) 7.75 V/m
(c) 1.73 V/m (d) 2.45 V/m

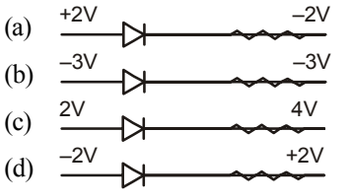
27. A 2V battery is connected across AB as shown in the figure. The value of the current supplied by the battery when in one case battery's positive terminal is connected to A and in other case when positive terminal of battery is connected to B will respectively be:
[Online April 11, 2015]



(a) 0.4 A and 0.2 A (b) 0.2 A and 0.4 A
(c) 0.1 A and 0.2 A (d) 0.2 A and 0.1 A

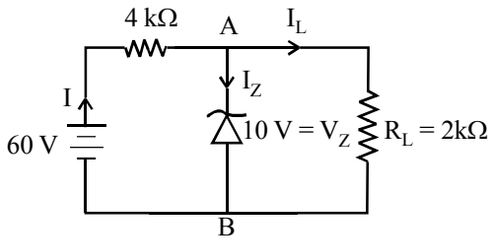
28. In an unbiased n-p junction electrons diffuse from n-region to p-region because : **[Online April 10, 2015]**
(a) holes in p-region attract them
(b) electrons travel across the junction due to potential difference
(c) only electrons move from n to p region and not the vice-versa
(d) electron concentration in n-region is more compared to that in p-region

29. The forward biased diode connection is: **[2014]**



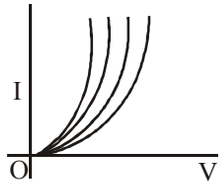
30. For LED's to emit light in visible region of electromagnetic light, it should have energy band gap in the range of:
[Online April 12, 2014]
(a) 0.1 eV to 0.4 eV (b) 0.5 eV to 0.8 eV
(c) 0.9 eV to 1.6 eV (d) 1.7 eV to 3.0 eV

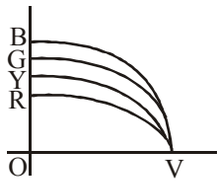
31. A Zener diode is connected to a battery and a load as show below: **[Online April 11, 2014]**



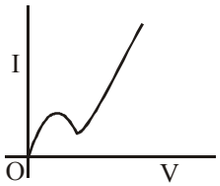
The currents, I, I_Z and I_L are respectively.
(a) 15 mA, 5 mA, 10 mA
(b) 15 mA, 7.5 mA, 7.5 mA
(c) 12.5 mA, 5 mA, 7.5 mA
(d) 12.5 mA, 7.5 mA, 5 mA

32. The I-V characteristic of an LED is **[2013]**

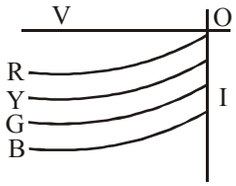
(a)


(b)


(c)

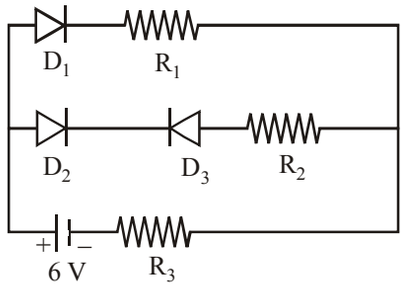


(d)



33. Figure shows a circuit in which three identical diodes are used. Each diode has forward resistance of 20 Ω and infinite backward resistance. Resistors $R_1 = R_2 = R_3 = 50\,\Omega$. Battery voltage is 6 V. The current through R_3 is :

[Online April 22, 2013]



(a) 50 mA (b) 100 mA
(c) 60 mA (d) 25 mA

34. This question has Statement 1 and Statement 2. Of the four choices given after the Statements, choose the one that best describes the two Statements.

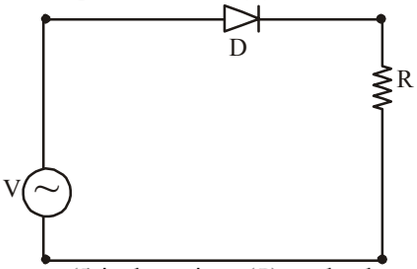
Statement 1: A pure semiconductor has negative temperature coefficient of resistance.

Statement 2: On raising the temperature, more charge carriers are released into the conduction band.

[Online May 12, 2012]

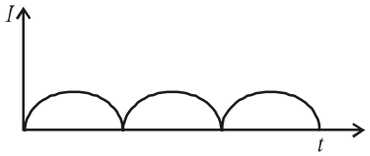
(a) Statement 1 is false, Statement 2 is true.
(b) Statement 1 is true, Statement 2 is false.
(c) Statement 1 is true, Statement 2 is true, Statement 2 is not a correct explanation of Statement 1.
(d) Statement 1 is true, Statement 2 is true, Statement 2 is the correct explanation of Statement 1.

35. A *p-n* junction (*D*) shown in the figure can act as a rectifier. An alternating current source (*V*) is connected in the circuit.

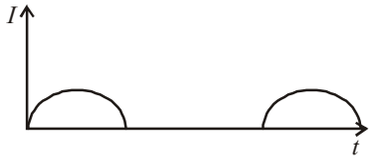


The current (*I*) in the resistor (*R*) can be shown by : **[2009]**

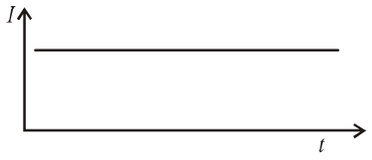
(a)



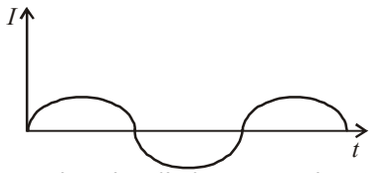
(b)



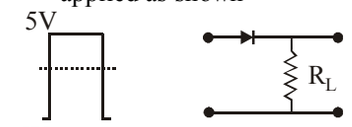
(c)



(d)

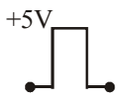


36. If in a *p-n* junction diode, a square input signal of 10 V is applied as shown **[2007]**

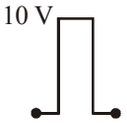


Then the output signal across R_L will be

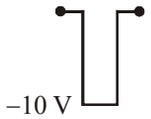
(a)



(b)



(c)

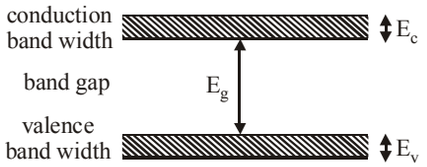


(d)

37. Carbon, silicon and germanium have four valence electrons each. At room temperature which one of the following statements is most appropriate ? **[2007]**

(a) The number of free electrons for conduction is significant only in Si and Ge but small in C.
(b) The number of free conduction electrons is significant in C but small in Si and Ge.
(c) The number of free conduction electrons is negligibly small in all the three.
(d) The number of free electrons for conduction is significant in all the three.

38. If the lattice constant of this semiconductor is decreased, then which of the following is correct? **[2006]**



(a) All E_c, E_g, E_v increase
(b) E_c and E_v increase, but E_g decreases
(c) E_c and E_v decrease, but E_g increases
(d) All E_c, E_g, E_v decrease

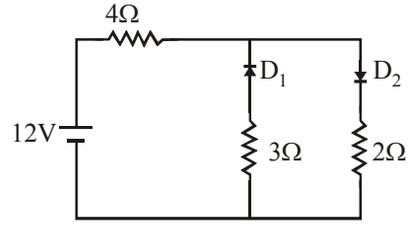
39. A solid which is not transparent to visible light and whose conductivity increases with temperature is formed by **[2006]**

(a) Ionic bonding
(b) Covalent bonding
(c) Vander Waals bonding
(d) Metallic bonding

40. If the ratio of the concentration of electrons to that of holes in a semiconductor is $\frac{7}{5}$ and the ratio of currents is $\frac{7}{4}$, then what is the ratio of their drift velocities? **[2006]**

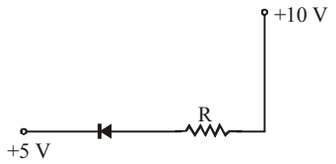
(a) $\frac{5}{8}$ (b) $\frac{4}{5}$ (c) $\frac{5}{4}$ (d) $\frac{4}{7}$

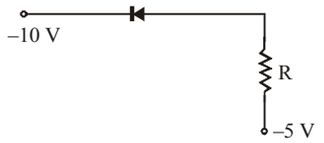
41. The circuit has two oppositively connected ideal diodes in parallel. What is the current flowing in the circuit? **[2006]**

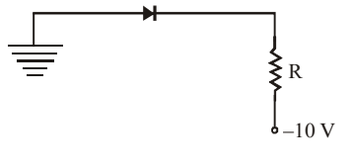


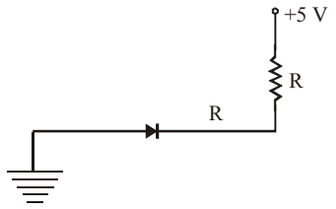
(a) 1.71A (b) 2.00A (c) 2.31A (d) 1.33A

42. In the following, which one of the diodes reverse biased? **[2006]**

(a)


(b)


(c)


(d)


43. The electrical conductivity of a semiconductor increases when electromagnetic radiation of wavelength shorter than 2480 nm is incident on it. The band gap in (eV) for the semiconductor is **[2005]**

(a) 2.5 eV (b) 1.1 eV (c) 0.7 eV (d) 0.5 eV

44. When p-n junction diode is forward biased then **[2004]**

(a) both the depletion region and barrier height are reduced
(b) the depletion region is widened and barrier height is reduced
(c) the depletion region is reduced and barrier height is increased
(d) Both the depletion region and barrier height are increased

45. A strip of copper and another of germanium are cooled from room temperature to 80K. The resistance of **[2003]**

(a) each of these decreases
(b) copper strip increases and that of germanium decreases
(c) copper strip decreases and that of germanium increases
(d) each of these increases

46. The difference in the variation of resistance with temeperature in a metal and a semiconductor arises essentially due to the difference in the **[2003]**

(a) crystal sturcture
(b) variation of the number of charge carriers with temperature
(c) type of bonding
(d) variation of scattering mechanism with temperature

47. In the middle of the depletion layer of a reverse- biased *p-n* junction, the **[2003]**

(a) electric field is zero
(b) potential is maximum
(c) electric field is maximum
(d) potential is zero

48. At absolute zero, Si acts as **[2002]**

(a) non-metal (b) metal
(c) insulator (d) none of these

49. By increasing the temperature, the specific resistance of a conductor and a semiconductor **[2002]**

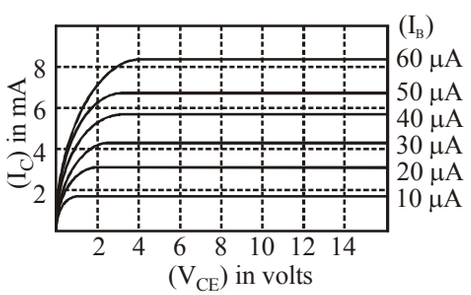
(a) increases for both (b) decreases for both
(c) increases, decreases (d) decreases, increases

50. The energy band gap is maximum in **[2002]**

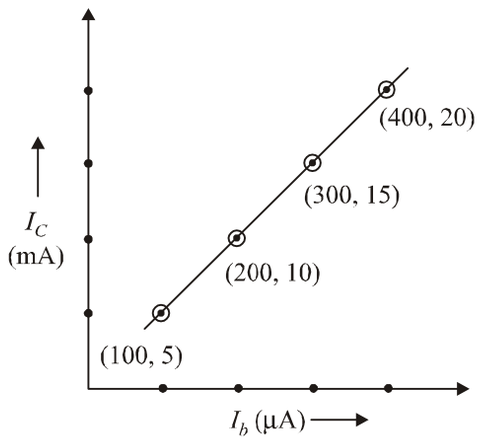
(a) metals (b) superconductors
(c) insulators (d) semiconductors.

TOPIC 2 Junction Transistor

51. The output characteristics of a transistor is shown in the figure. When V_{CE} is 10 V and $I_C = 4.0$ mA, then value of β_{ac} is _____. **[NA Sep. 06, 2020 (II)]**



52. The transfer characteristic curve of a transistor, having input and output resistance 100 Ω and 100 k Ω respectively, is shown in the figure. The Voltage and Power gain, are respectively : **[12 Apr. 2019 I]**



(a) $2.5\times10^4, 2.5\times10^6$ (b) $5\times10^4, 5\times10^6$
(c) $5\times10^4, 5\times10^5$ (d) $5\times10^4, 2.5\times10^6$

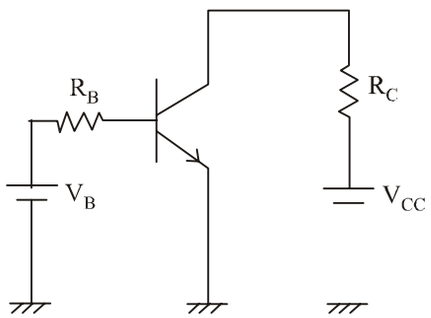
53. An npn transistor operates as a common emitter amplifier, with a power gain of 60 dB. The input circuit resistance is 100Ω and the output load resistance is 10 kΩ. The common emitter current gain β is : **[10 Apr. 2019 I]**

(a) 10^2 (b) 60 (c) 6×10^2 (d) 10^4

54. An NPN transistor is used in common emitterconfiguration as an amplifier with 1 k &! load resistance. Signal voltage of 10 mV is applied across the base-emitter. This produces a 3 mA change in the collector current and 15 ¼A change in the base current of the amplifier. The input resistance and voltage gain are: **[9 April 2019 I]**

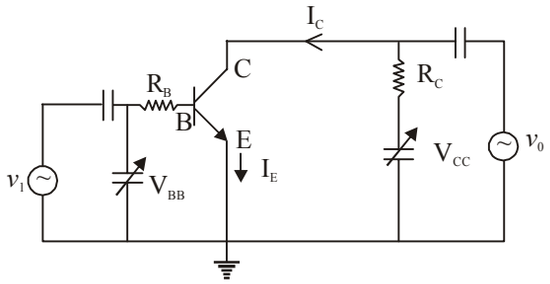
(a) 0.33 k Ω 1.5 (b) 0.67 k Ω 300
(c) 0.67 k Ω 200 (d) 0.33 k Ω 300

55. A common emitter amplifier circuit, built using an npn transistor, is shown in the figure. Its dc current gain is 250, $R_C = 1$ k &! and $V_{CC} = 10$V. What is the minimum base current for V_{CE} to reach saturation ? **[8 Apr. 2019 II]**



(a) 40 μA (b) 100 μA
(c) 7 μA (d) 10 μA

56.



In the figure, given that V_{BB} supply can vary from 0 to 5.0 V, V_{CC} = 5 V, $\beta_{dc} = 200$, $R_B = 100$ kΩ, $R_C = 1$ KΩ and $V_{BE} = 1.0$ V. The minimum base current and the input voltage at which the transistor will go to saturation, will be, respectively : **[12 Jan. 2019 II]**

(a) 25 μA and 3.5 V (b) 20 μA and 3.5 V
(c) 25 μA and 2.8 V (d) 20 μA and 2.8 V

57. In a common emitter configuration with suitable bias, it is given than R_L is the load resistance and R_{BE} is small signal dynamic resistance (input side). Then, voltage gain, current gain and power gain are given, respectively, by:
(β is current gain, I_B, I_C, I_E are respectively base, collector and emitter currents:) **[Online April 15, 2018]**

(a) $\beta\frac{R_L}{R_{BE}}, \frac{\Delta I_E}{\Delta I_B}, \beta^2\frac{R_L}{R_{BE}}$

(b) $\beta^2\frac{R_L}{R_{BE}}, \frac{\Delta I_C}{\Delta I_B}, \beta\frac{R_L}{R_{BE}}$

(c) $\beta^2\frac{R_L}{R_{BE}}, \frac{\Delta I_C}{\Delta I_E}, \beta^2\frac{R_L}{R_{BE}}$

(d) $\beta\frac{R_L}{R_{BE}}, \frac{\Delta I_C}{\Delta I_B}, \beta^2\frac{R_L}{R_{BE}}$

58. The current gain of a common emitter amplifier is 69. If the emitter current is 7.0 mA, collector current is : **[Online April 9, 2017]**

(a) 9.6 mA (b) 6.9 mA
(c) 0.69 mA (d) 69 mA

59. In a common emitter amplifier circuit using an n-p-n transistor, the phase difference between the input and the output voltages will be : **[Online April 2, 2017]**

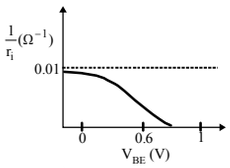
(a) 135° (b) 180°
(c) 45° (d) 90°

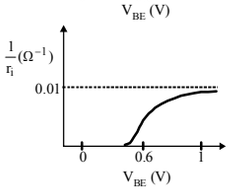
60. For a common emitter configuration, if α and β have their usual meanings, the incorrect relationship between α and β is : **[2016]**

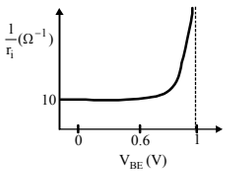
(a) $a = \frac{b}{1+b}$ (b) $a = \frac{b^2}{1+b^2}$

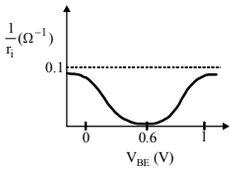
(c) $\frac{1}{a} = \frac{1}{b} + 1$ (d) None of these

61. A realistic graph depicting the variation of the reciprocal of input resistance in an input characteristics measurement in a common emitter transistor configuration is : **[Online April 10, 2016]**

(a) 

(b) 

(c) 

(d) 

62. The ratio (R) of output resistance r_0, and the input resistance r_i in measurements of input and output characteristics of a transistor is typically in the range : **[Online April 10, 2016]**

(a) $R \sim 10^2 - 10^3$ (b) $R \sim 1 - 10$
(c) $R \sim 0.1 - 1.0$ (d) $R \sim 0.1 - 0.01$

63. An unknown transistor needs to be identified as a npn or pnp type. A multimeter, with +ve and –ve terminals, is used to measure resistance between different terminals of transistor. If terminal 2 is the base of the transistor then which of the following is correct for a pnp transistor? **[Online April 9, 2016]**

(a) +ve terminal 2, –ve terminal 3,resistance low
(b) +ve terminal 2, –ve terminal 1, resistane high
(c) +ve terminal 1, –ve terminal 2, resistance high
(d) +ve terminal 3, –ve terminal 2, resistance high

64. An n-p-n transistor has three leads A, B and C. Connecting B and C by moist fingers, A to the positive lead of an ammeter, and C to the negative lead of the ammeter, one finds large deflection. Then, A, B and C refer respectively to: **[Online April 9, 2014]**

(a) Emitter, base and collector
(b) Base, emitter and collector
(c) Base, collector and emitter
(d) Collector, emitter and base.

65. A working transistor with its three legs marked *P*, *Q* and *R* is tested using a multimeter. No conduction is found between *P* and *Q*. By connecting the common (negative) terminal of the multimeter to *R* and the other (positive) terminal to *P* or *Q*, some resistance is seen on the multimeter. Which of the following is true for the transistor? **[2008]**

(a) It is an npn transistor with *R* as base
(b) It is a pnp transistor with *R* as base
(c) It is a pnp transistor with *R* as emitter
(d) It is an npn transistor with *R* as collector

66. In a common base mode of a transistor, the collector current is 5.488 mA for an emitter current of 5.60 mA. The value of the base current amplification factor (β) will be **[2006]**

(a) 49 (b) 50
(c) 51 (d) 48

67. In a common base amplifier, the phase difference between the input signal voltage and output voltage is **[2005]**

(a) π (b) $\frac{\pi}{4}$
(c) $\frac{\pi}{2}$ (d) 0

68. When npn transistor is used as an amplifier **[2004]**

(a) electrons move from collector to base
(b) holes move from emitter to base
(c) electrons move from base to collector
(d) holes move from base to emitter

69. For a transistor amplifier in common emitter configuration for load impedance of 1k Ω $(h_{fe} = 50$ and $h_{oe} = 25)$ the current gain is **[2004]**

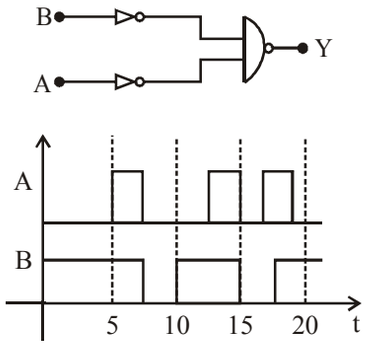
(a) –24.8 (b) –15.7
(c) –5.2 (d) –48.78

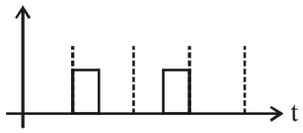
70. The part of a transistor which is most heavily doped to produce large number of majority carriers is **[2002]**

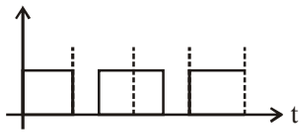
(a) emmiter
(b) base
(c) collector
(d) can be any of the above three.

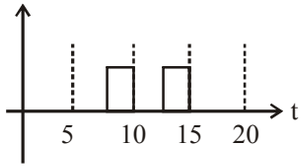
TOPIC 3 Digital Electronics and Logic Gates

71. Identify the correct output signal Y in the given combination of gates (as shown) for the given inputs A and B. **[Sep. 06, 2020 (I)]**



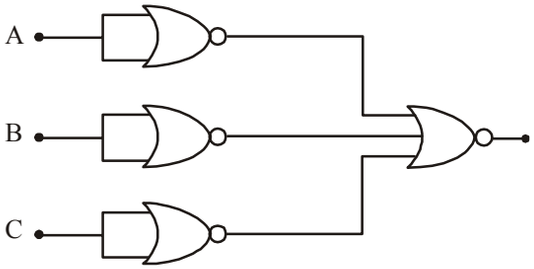
(a)


(b)


(c)


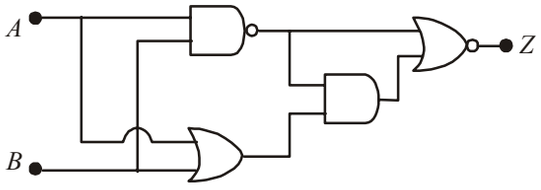
(d)


72. Identify the operation performed by the circuit given below:
[Sep. 04, 2020 (II)]



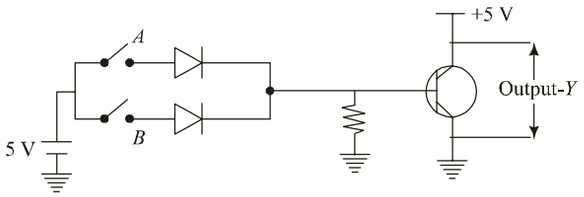
(a) NAND (b) OR
(c) AND (d) NOT

73. In the following digitial circuit, what will be the output at 'Z', when the input (A, B) are (1, 0), (0, 0), (1, 1), (0, 1) :
[Sep. 02, 2020 (II)]



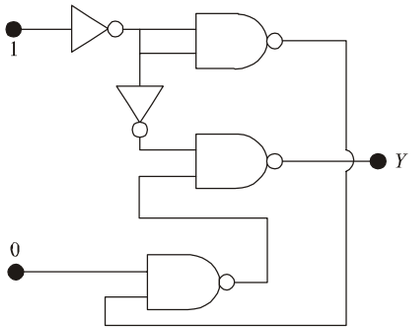
(a) 0, 0, 1, 0 (b) 1, 0, 1, 1
(c) 1, 1, 0, 1 (d) 0, 1, 0, 0

74. Boolean relation at the output stage-Y for the following circuit is: **[8 Jan. 2020 I]**



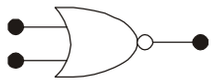
(a) $\overline{A}+\overline{B}$ (b) $A+B$
(c) $A.B$ (d) $\overline{A}.\overline{B}$

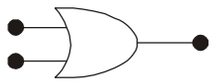
75. In the given circuit, value of Y is: **[8 Jan. 2020 II]**

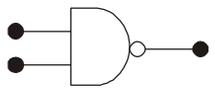


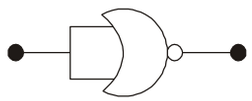
(a) 0
(b) toggles between 0 and 1
(c) will not execute
(d) 1

76. Which of the following gives a reversible operation?
[7 Jan. 2020 I]

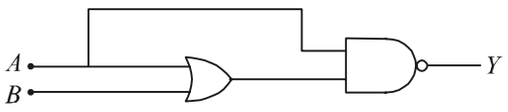
(a)


(b)


(c)


(d)


77. The truth table for the circuit given in the fig. is :
[9 April 2019 I]



(a)

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	1

(b)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

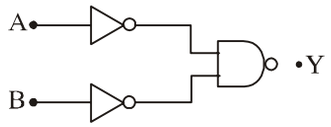
(c)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

(d)

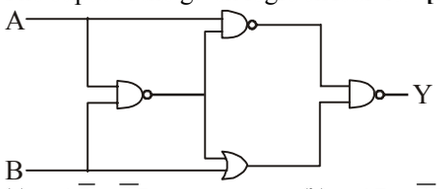
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

78. The logic gate equivalent to the given logic circuit is:
[9 Apr. 2019 II]



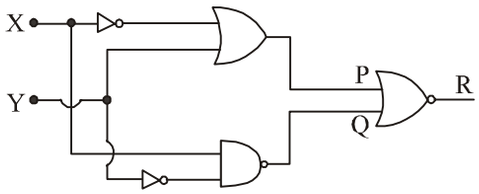
(a) NAND (b) OR (c) NOR (d) AND

79. The ouput of the given logic cirfcuit is: **[12 Jan. 2019 I]**



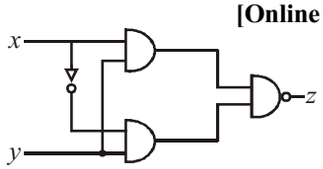
(a) $A\bar{B} + \bar{A}B$ (b) $AB + \bar{A}B$
(c) $A\bar{B}$ (d) $\bar{A}B$

80. To get output '1' at R, for the given logic gate circuit the input values must be: **[10 Jan. 2019 I]**



(a) X = 0, Y = 1 (b) X = 1, Y = 1
(c) X = 1, Y = 0 (d) X = 0, Y = 0

81. Truth table for the given circuit will be
[Online April 15, 2018]



(a)

x	y	z
0	0	1
0	1	1
1	0	1
1	1	0

(b)

x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

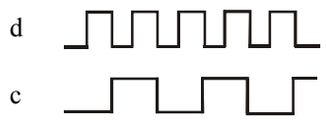
(c)

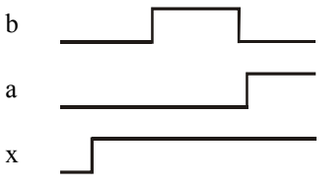
x	y	z
0	0	1
0	1	1
1	0	1
1	1	1

(d)

x	y	z
0	0	0
0	1	1
1	0	1
1	1	1

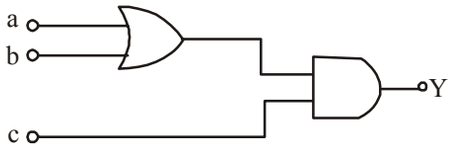
82. If a, b, c, d are inputs to a gate and x is its output, then, as per the following time graph, the gate is : **[2016]**





(a) OR (b) NAND
(c) NOT (d) AND

83. To get an output of 1 from the circuit shown in figure the input must be : **[Online April 10, 2016]**



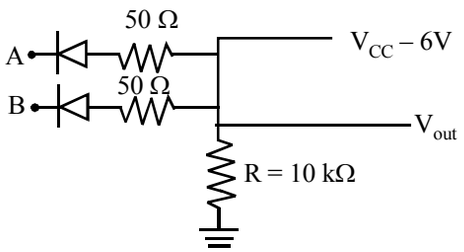
(a) a = 0, b = 0, c = 1 (b) a = 1, b = 0, c = 0
(c) a = 1, b = 0, c = 1 (d) a = 0, b = 1, c = 0

84. The truth table given in fig. represents :
[Online April 9, 2016]

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(a) OR – Gate (b) NAND– Gate
(c) AND– Gate (d) NOR– Gate

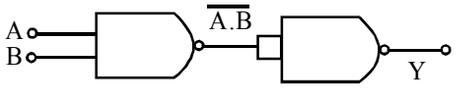
85.



Given: A and B are input terminals.
Logic 1 = > 5 V
Logic 0 = < 1 V
Which logic gate operation, the above circuit does?
[Online April 19, 2014]

(a) AND Gate (b) OR Gate
(c) XOR Gate (d) NOR Gate

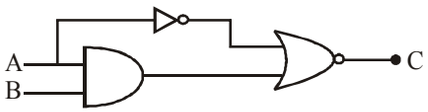
86. Identify the gate and match A, B, Y in bracket to check.
[Online April 9, 2014]

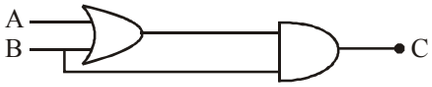


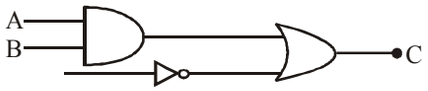
(a) AND (A = 1, B = 1, Y = 1)
(b) OR (A = 1, B = 1, Y = 0)
(c) NOT (A = 1, B = 1, Y = 1)
(d) XOR (A = 0, B = 0, Y = 0)

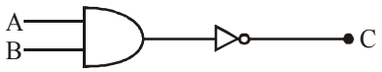
87. Which of the following circuits correctly represents the following truth table ? **[Online April 25, 2013]**

A	*B*	*C*
0	0	0
0	1	0
1	0	1
1	1	0

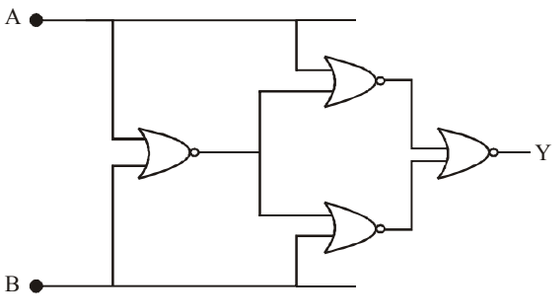
(a) 

(b) 

(c) 

(d) 

88. A system of four gates is set up as shown. The 'truth table' corresponding to this system is : **[Online April 23, 2013]**



(a)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(b)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	0

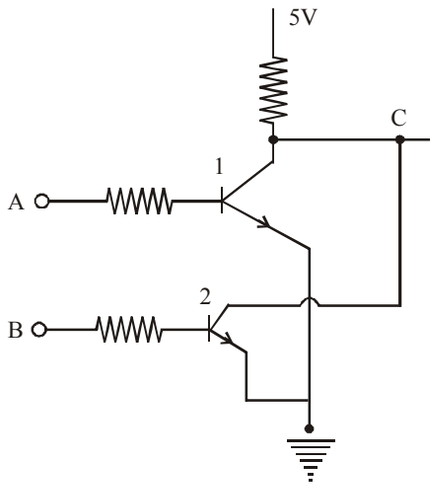
(c)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

(d)

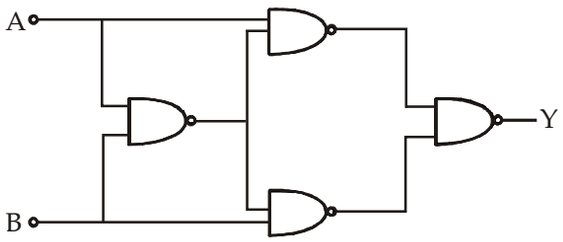
A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

89. Consider two *npn* transistors as shown in figure. If 0 Volts corresponds to false and 5 Volts correspond to true then the output at C corresponds to : **[Online April 9, 2013]**



(a) A NAND B (b) A OR B
(c) A AND B (d) A NOR B

90. Truth table for system of four NAND gates as shown in figure is : **[2012]**



(a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(b)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

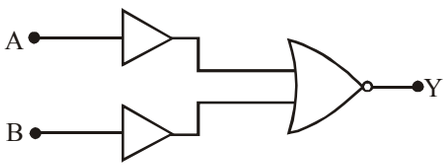
(c)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

(d)

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

91. The figure shows a combination of two NOT gates and a NOR gate. **[Online May 26, 2012]**



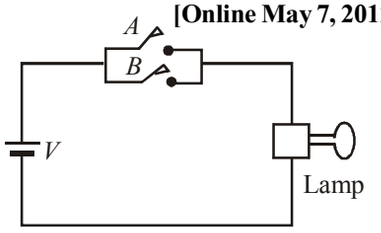
The combination is equivalent to a
(a) NAND gate (b) NOR gate
(c) AND gate (d) OR gate

92. Which one of the following is the Boolean expression for NOR gate? **[Online May 19, 2012]**

(a) $Y = \overline{A + B}$ (b) $Y = \overline{A.B}$

(c) $Y = A.B$ (d) $Y = \overline{A}$

93. Which logic gate with inputs A and B performs the same operation as that performed by the following circuit? **[Online May 7, 2012]**



(a) NAND gate

(b) OR gate

(c) NOR gate

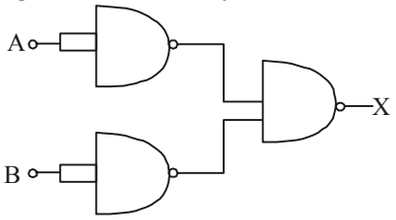
(d) AND gate

94. The output of an OR gate is connected to both the inputs of a NAND gate. The combination will serve as a: **[2011 RS]**

(a) NOT gate (b) NOR gate

(c) AND gate (d) OR gate

95. The combination of gates shown below yields **[2010]**



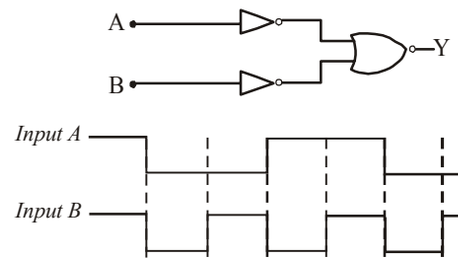
(a) OR gate

(b) NOT gate

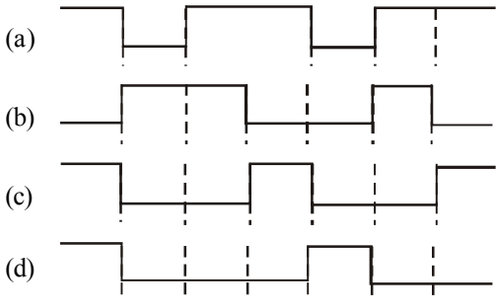
(c) XOR gate

(d) NAND gate

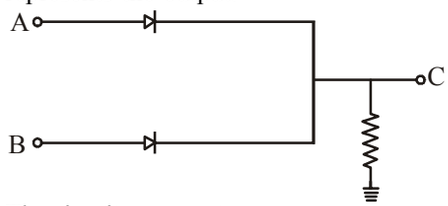
96. The logic circuit shown below has the input waveforms 'A' and 'B' as shown. Pick out the correct output waveform. **[2009]**



Output is



97. In the circuit below, A and B represent two inputs and C represents the output. **[2008]**



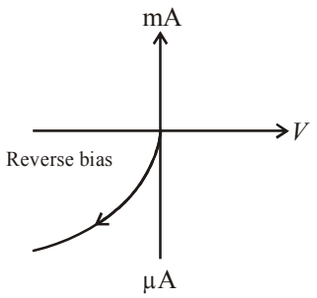
The circuit represents

(a) NOR gate (b) AND gate

(c) NAND gate (d) OR gate

Hints & Solutions

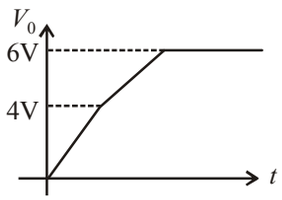
1. **(d)** I-V characteristic of a photodiode is as follows :



On increasing the biasing voltage of a photodiode, the magnitude of photocurrent first increases and then attains a saturation.

2. **(c)** Till input voltage reaches 4 V. No zener is in breakdown region so $V_0 = V_i$. Then now when V_i changes between 4 V to 6 V one zener with 4 V will breakdown and P.D. across this zener will become constant and remaining potential will dorp across resistance in series with 4 V zener.

Now current in circuit increases abruptly and source must have an internal resistance due to which some potential will get drop across the source also so correct graph between V_0 and t will be



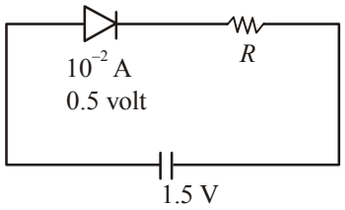
3. **(c)** Here two zener diodes are in reverse polarity so if one is in forward bias the other will be in reverse bias and above 6V the reverse bias will too be in conduction mode. Hence when V > 6V the output will be constant. And when V < 6V it will follow the inut voltage.

4. **(c)** According to question, when diode is forward biased,

$V_{diode} = 0.5$ V

Safe limit of current, $I = 10$ mA $= 10^{-2}$ A

$R_{min} = ?$



Voltage through resistance

$V_R = 1.5 - 0.5 = 1$ volt

$iR = 1 (= V_R)$

$\therefore R_{min} = \frac{1}{i} = \frac{1}{10^{-2}} = 100\ \Omega$

5. **(d)** Given,

Wavelength of photon, $\lambda = 400$ nm

A photodiode can detect a wavelength corresponding to the energy of band gap. If the signal is having wavelength greater than this value, photodiode cannot detect it.

$\therefore$ Band gap $E_g = \frac{hc}{\lambda} = \frac{1237.5}{400} = 3.09$ eV

6. **(12)** Right hand diode is reversed biased and left hand diode is forward biased.

Hence Voltage at 'A'

$V_A = 12.7 - 0.7 = 12$ volt

7. **(c)** Both the diodes are reverse biased, so, there is no flow of current through 5Ω and 20Ω resistances.

Now, two resistors of 10Ω and two resistors of 5Ω are in series.

Hence current I through the network = 0.3 A

8. **(c)** In case I diode is reverse biased, so no current flows

$\therefore \quad Q_A = CV$

In case II, current will flow as diode is forward biased. So, it offers negligible resistance to the flow of current and thus be replaced by short circuit. Now, the charge of capacitor will leak through the resistance and decay exponentially with time.

During discharging of capacitor

Potential difference across the capacitor at any instant

$V' = Ve^{-\frac{t}{CR}}$

But $t = CR$

$V' = Ve^{-1} = \frac{V}{e}$

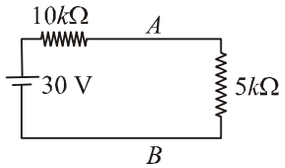
$\therefore \quad$ Charge $Q_B = CV' = \frac{CV}{e}$

9. **(40)** Current in the circuit, $I = \frac{12-8}{400} = 10^{-2}\ A$

Power dissipited in each diode, $P = VI$

$\Rightarrow \quad P = 4 \times 10^{-2} = 40\ mW$

10. **(a)** The given circuit has two $10k\Omega$ resistances in parallel, so we can reduce this parallel combination to a single equivalent resistance of $5k\Omega$.



Diode is in forward bias. So it will behave like a conducting wire.

$$V_A - V_B = \frac{30}{5+10} \times 5 = 10\,V$$

11. **(d)** Current in load resistance,

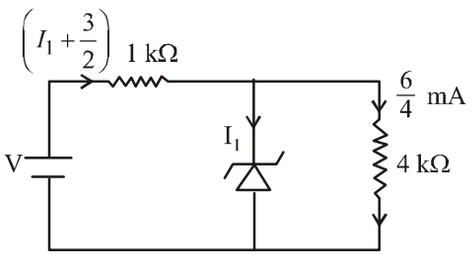
$$i_1 = \frac{6}{4\times10^3} = 1.5 \times 10^{-3}\,A = 1.5\,mA$$

For $V = 16$ volt,

$$i_s = \frac{(16-6)}{2\times10^3} = 5\,mA$$

$$\therefore \quad i_2 = i_s - i_1 = 5 - 1.5 = 3.5\,mA$$

12. **(c)**



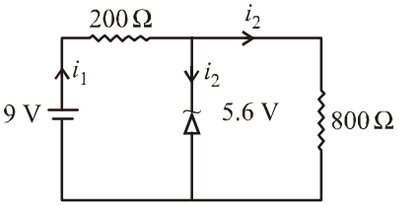
For voltage, V = 8V

$$\text{Current, } I_1 = \left(8-6-\frac{3}{2}\right) = \frac{1}{2} = 0.5\,mA$$

For voltage, V = 16V

$$\text{Current, } I_2 = \left(16-6-\frac{3}{2}\right) = 8.5\,mA$$

13. **(a)**



P.D. across 800Ω resistors = 5.6 V

$$\text{so, } I_{800\Omega} = \frac{5.6}{800} A = 7\,mA$$

Now, P.D. across 200Ω resistors = 9 – 5.6 V = 3.4 V

$$\text{so, } I_{200\Omega} = \frac{9-5.6}{200} = 17\,mA$$

so, current through zener diode = I_2 = 17 – 7 = 10 mA

14. **(a)** Since voltage across zener diode does not reach to breakdown voltage therefore its resistance will be infinite & current through it is 0.

15. **(b)** As D_2 is reversed biased, so no current through 75Ω resistor.

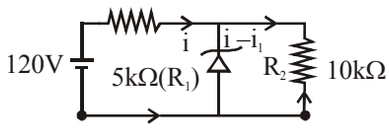
now $R_{eq} = 150 + 50 + 100$

$= 300\,\Omega$

$$\text{So, required current } I = \frac{\text{BatteryVoltage}}{300}$$

$$I = \frac{6}{300} = 0.02$$

16. **(a)** The voltage across zener diode is constant



$$i_{(R_2)} = \frac{V}{R} = \frac{50}{10\times10^3} = 5\times10^{-3}\,A$$

$$i_{(R_1)} = \frac{V}{R} = \frac{120-50}{5\times10^3} = \frac{70}{5\times10^3} 14\times10^{-3}\,A$$

$$\therefore i_{zenerdiode} = 14\times10^{-3} - 5\times10^{-3} = 9\times10^{-3}\,A = 9\,mA$$

17. **(c)** As we know, current density,

$$j = \sigma E = nev_d$$

$$\sigma = ne\frac{v_d}{E} = ne\mu$$

$$\frac{1}{\sigma} = \rho = \frac{1}{n_e e \mu_e} = \text{Resistivity}$$

$$= \frac{1}{10^{19}\times1.6\times10^{19} - 19\times1.6}$$

or $P = 0.4\,\Omega m$

18. **(d)** Initially Ge and Si are both forward biased so current will effectivily pass through Ge diode $\therefore V_\circ = 12 - 0.3 = 11.7$ V

And if "Ge" is revesed then current will flow through "Si" diode

$\therefore V_\circ = 12 - 0.7 = 11.3$ V

Clearly, $V_\circ$ changes by 11.7 – 11.3 = 0.4 V

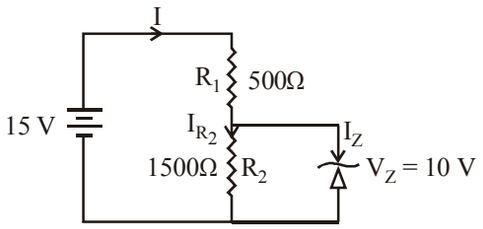
19. **(c)** Clearly from fig. given in question, Silicon diode is in forward bias.

$\therefore$ Potential barrier across diode

$\Delta V = 0.7$ volts

$$\text{Current, } I = \frac{V - \Delta V}{R} = \frac{3-0.7}{200} = \frac{2.3}{200} = 11.5mA$$

20. **(b)**



The voltage drop across R_2 is $V_{R_2} = V_Z = 10\,V$

The current through R_2 is

$$I_{R_2} = \frac{V_{R_2}}{R_2} = \frac{10\,V}{1500\Omega} = 0.667 \times 10^{-2}\,A$$

$$= 6.67 \times 10^{-3}\,A = 6.67\,mA$$

The voltage drop across R_1 is

$$V_{R_1} = 15V - V_{R_2} = 15V - 10V = 5V$$

The current through R_1 is

$$I_{R_1} = \frac{V_{R_1}}{R_1} = \frac{5\,V}{500\Omega} = 10^{-2}\,A = 10 \times 10^{-3}\,A = 10\,mA$$

The current through the zener diode is

$$I_Z = I_{R_1} - I_{R_2} = (10 - 6.67)mA = 3.3\,mA$$

21. **(a)** The conductivity of semiconductor

$$\sigma = e\,(\eta_e\mu_e + \eta_h\mu_h)$$

$$= 1.6 \times 10^{-19}(5 \times 10^{18} \times 2 + 5 \times 10^{19} \times 0.01)$$

$$= 1.6 \times 1.05 = 1.68$$

22. **(b)** Forward bias resistance $= \frac{\Delta V}{\Delta I} = \frac{0.1}{10 \times 10^{-3}} = 10\,\Omega$

Reverse bias resistance $= \frac{10}{10^{-6}} = 10^7\,\Omega$

Ratio of resistances $= \frac{\text{Forward bias resistance}}{\text{Reverse bias resistance}} = 10^{-6}$

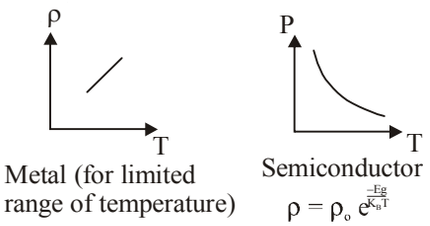
23. **(c)** Graph (p) is for a simple diode.

Graph (q) is showing the V Break down used for zener diode.

Graph (r) is for solar cell which shows cut-off voltage and open circuit current.

Graph (s) shows the variation of resistance h and hence current with intensity of light.

24. **(a)**



Metal (for limited range of temperature)

Semiconductor $\rho = \rho_o\, e^{\frac{-E_g}{K_B T}}$

25. **(c)** The minimum voltage range of DC source is given by

$V^2 = PR \quad \because P = 1$ watt, $R = 100\Omega$

$= 1 \times 100$

$\therefore V = 10$ volt.

26. **(d)** Using $U_{av} = \frac{1}{2}\varepsilon_0 E_0^{\,2}$

But $U_{av} = \frac{P}{4\pi r^2 \times c}$

$$\therefore \quad \frac{P}{4\pi r^2} = \frac{1}{2}\varepsilon_0 E_0^{\,2} \times c$$

$$E_0^2 = \frac{2P}{4\pi r^2 \varepsilon_0 c} = \frac{2 \times 0.1 \times 9 \times 10^9}{1 \times 3 \times 10^8}$$

$\therefore \quad E_0 = \sqrt{6} = 2.45 V/m$

27. **(a)** When positive terminal connected to A then diode D_1 is forward biased, current, $I = \frac{2}{5} = 0.4A$

When positive terminal connected to B then diode D_2 is forward biased, current, $I = \frac{2}{10} = 0.2A$

$$E_0^2 = \frac{2P}{4\pi r^2 \varepsilon_0 c} = \frac{2 \times 0.1 \times 9 \times 10^9}{1 \times 3 \times 10^8}$$

$\therefore \quad E_0 = \sqrt{6} = 2.45 V/m$

28. (d) Electrons in an unbiased *p-n* junction, diffuse from *n* -region i.e. higher electron concentration to *p*-region i.e. low electron concentration region.

29. **(a)**

For forward bias, p-side must be at higher potential than *n*-side. $\Delta V = (+)Ve$

30. **(d)** Energy band gap range is given by,

$$E_g = \frac{hc}{\lambda}$$

For visible region $\lambda = \left(4 \times 10^{-7} \sim 7 \times 10^{-7}\right)m$

$$E_g = \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{7 \times 10^{-7}}$$

$$= \frac{19.8 \times 10^{-26}}{7 \times 10^{-7}}$$

$$= \frac{2.8 \times 10^{-19}}{1.6 \times 10^{-19}}$$

$E_g = 1.75\,eV$

31. **(d)** Here, $R = 4\,k\Omega = 4 \times 10^3\,\Omega$

$V_i = 60\,V$

Zener voltage $V_z = 10\,V$

$R_L = 2\,k\Omega = 2 \times 10^3\,\Omega$

Load current, $I_L = \frac{V_Z}{R_L} = \frac{10}{2 \times 10^3} = 5\,mA$

Current through R, $I = \frac{V_i - V_Z}{R}$

$= \frac{60-10}{4 \times 10^3} = \frac{50}{4 \times 10^3} = 12.5\,mA$

Fom circuit diagram,

$I = I_Z + I_L$

$\Rightarrow \quad 12.5 = I_Z + 5$

$\Rightarrow \quad I_Z = 12.5 - 5 = 7.5\,mA$

32. **(a)** For same value of current higher value of voltage is required for higher frequency hence (a) is correct answer.

33. **(a)** Here, diodes D_1 and D_2 are forward biased and D_3 is reverse biased.

Therefore current through R_3

$i = \frac{V}{R'} = \frac{6}{120} = \frac{1}{20}A = 50\,mA$

34. **(d)** Temperature coefficient of resistance is negative for pure semiconductor. And no. of charge carriers in conduction band increases with increase in temperature.

35. **(b)** The given circuit will work as half wave rectifier as it conducts during the positive half cycle of input AC.

Forward biased in one half cycle and reverse biased in the other half cycle].

36. **(a)** The current will flow through R_L when the diode is forward biased.

37. **(a)** Si and Ge are semiconductors but C is an insulator. In Si and Ge at room temperature, the energy band gap is low due to which electrons in the covalent bonds gains kinetic energy and break the bond and move to conduction band. As a result, hole is created in valence band. So, the number of free electrons is significant in Si and Ge.

38. **(c)** A crystal structure is made up of a unit cell arranged in a particular way; which is periodically repeated in three dimensions on a lattice. The spacing between unit cells in various directions is called its lattice constants. As lattice constants increases the band-gap (E_g), also increases which means more energy would be required by electrons to reach the conduction band from the valence band. Automatically E_c and E_v decreases.

39. **(b)** Van der Waal's bonding is attributed to the attractive forces between molecules of a liquid. The conductivity of semiconductors (covalent bonding) and insulators (ionic bonding) increases with increase in temperature.

Solid which is formed by covalent bond is not transparent to visible light and its conductivity increase with temperature.

40. **(c)** Relation between drift velocity and current is

$I = nAeV_d$

$\frac{I_e}{I_h} = \frac{n_e e A v_e}{n_h e A v_h}$

$\Rightarrow \frac{7}{4} = \frac{7}{5} \times \frac{v_e}{v_h}$

$\Rightarrow \frac{v_e}{v_h} = \frac{5}{4}$

41. **(b)** D_2 is forward biased.

D_1 is reversed biased. So, it will act like an open circuit.

So effective resistance of the circuit

$R = 4 + 2 = 6\Omega \qquad \therefore i = \frac{E}{R} = \frac{12}{6} = 2\ A$

42. **(d)** p-side connected to low potential and n-side is connected to high potential.

43. **(d)** Band gap = energy of photon of wavelength 2480 nm. So,

Band gap, $E_g = \frac{hc}{\lambda}$

$= \left(\frac{6.63 \times 10^{-34} \times 3 \times 10^8}{2480 \times 10^{-9}} \right) \times \frac{1}{1.6 \times 10^{-19}} eV$

$= 0.5\,eV$

44. **(a)** In forward biasing, the p type is connected to positive terminal and n type is connected with negative terminal. So holes from p region and electron from n region are pushed towards the Junction which reduces the width of depletion layer. Also, distance between diffused holes and electrons decrease, which decrease electric field hence barrier potential.

45. **(c)** Copper is a conductor and in conductor resistance decreases with decrease in temperature. Germanium is a semicon ductor. In semi-conductor resistance increases with decrease in temperature.

46. **(b)** When the temperature increases, certain bounded electrons become free which tend to promote conductivity. Simultaneously number of collisions between electrons and positive kernels increases which decrease the relaxation time.

47. **(a)** In reverse biasing the width of depletion region increases, and current flowing through diode is zero. Thus, electric field is zero at middle of depletion region.

48. **(c)** Pure silicon, at OK, will contain all the electrons in bounded state. The conduction band will be empty. So there will be no free electrons (in conduction band) and holes (in valence band).Therefore no electrons from valence band are able to shift to conduction band due to thermal agitation. Pure silicon will act as insulator.

49. **(c)** Specific resistance (resistivity) is given by

$$\rho = \frac{m}{ne^2\tau}$$

where n = no. of free electrons per unit volume

and τ = average relaxation time

For a conductor with rise in temperature n increases. Increase in temperature results increase in number of collision between free electrons due to which relaxation time T decreases. But the decrease in τ is more dominant than increase in n resulting an increase in the value of ρ .

For a semiconductor with rise in temperature, n increases and τ decreases. But the increase in n is more dominant than decrease in τ resulting in a decrease in the value of ρ.

ALTERNATE SOLUTION

$\rho_2 = \rho_1(1+\alpha\Delta T)$

For conductor α is positive

$\therefore \rho_2 > \rho_1$ for ΔT positive i.e., increase in temperature.

For semi conductor α is negative

$\therefore \rho_2 < \rho_1$ for ΔT positive.

50. **(c)** In insulators, valence band is completely filled while conduction band is empty. The energy band gap is maximum in insulators.

51. **(150)**

At $V_{CE} = 10$ V and $I_C = 4$ mA

Change in base current, $\Delta I_B = (30-20) = 10\ \mu A$

Change in collector current, $\Delta I_C = (4.5-3) = 1.5$ mA

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right) = \frac{1.5\ mA}{10\mu A} = 150$$

52. **(Bonus)** $\beta = \frac{\Delta i_c}{\Delta i_b} = \frac{200-100}{10-5} = 20$

$$\text{Voltage gain} = \beta\frac{R_2}{R_1} = \frac{20\times100\times10^3}{100} = 20\times10^3$$

$$\text{Power gain} = \beta^2\frac{R_2}{R_1} = 20^2\left(\frac{100\times10^3}{100}\right) = 4\times10^5$$

53. **(a)** Power gain $= 60 = 10\log\left(\frac{P_0}{p_i}\right)$

$$\Rightarrow 6 = \log\left(\frac{P_0}{p_i}\right)$$

$$\Rightarrow \frac{P_0}{p_i} = 10^6$$

$$= \beta^2\left(\frac{R_{out}}{R_{in}}\right)$$

$$\Rightarrow 10^6 = \beta^2\left(\frac{10000}{100}\right) \quad [\text{as } R_{out} = 10,000\Omega\ R_{in} = 100\Omega]$$

$$\Rightarrow \beta = 100$$

54. **(b)** $\beta = \frac{\Delta lc}{\Delta lb} = \frac{3\times10^{-3}}{15\times10^{-6}} = 200$

We have $\frac{V_0}{V_i} = \beta\frac{R^2}{R_1}$

or $\frac{V_0}{V_i} = 200\left(\frac{1000}{R_1}\right)$

If $R_1 = 0.67\text{k}\Omega \Rightarrow \frac{V_0}{V_i} = 300$

55. **(a)** Given, $\beta = 250$

Voltage gain, $\frac{V_{CC}}{V_B} = \beta\frac{R_C}{R_B}$

$$\frac{10}{V_B} = 250\times\frac{10^3}{R_B}$$

$$\therefore \frac{V_B}{R_B} = \frac{1}{25\times10^3} = 40\mu A$$

56. **(a)** At saturation, $V_{CE} = 0$

$$V_{CE} = V_{CC} - I_C R_C$$

$$\Rightarrow \quad I_C = \frac{V_{CC}}{R_c} = 5\times10^{-3}\text{ A}$$

Current gain,

$$\beta_{dc} = \frac{I_C}{I_B}$$

$$I_B = \frac{5\times10^{-3}}{200} = 25\ \mu A$$

At input side

$$V_{BB} = I_B R_B + V_{BE}$$
$$= (25\text{ mA})(100\text{ k}\Omega) + 1\text{V}$$
$$V_{BB} = 3.5\text{ V}$$

57. **(d)** Curent gain $\beta = \frac{\Delta I_C}{I_B}$

Voltage gain A_v = Current gain × Resistance gain $= \beta\frac{R_L}{R_{BE}}$

Power gain A_p = (Current gain)^2 × Resistance gain

$$= \beta^2\frac{R_L}{R_{BE}}$$

58. **(b)** Given, current gain of CE amplifier $\beta = 69$, $I_E = 7$ mA

or $\frac{I_C}{I_B} = 69$

We know that, $\alpha = \frac{\beta}{1+\beta} = \frac{69}{70} = \frac{I_C}{I_E}$

$I_C = I_E \times \frac{69}{70} = \frac{69}{70} \times 7$

Collector current, $I_C = 6.9$ mA

59. **(b)** In common emitter configuration for *n-p-n* transistor input and output signals are 180° out of phase *i.e.,* phase difference between output and input voltage is 180°.

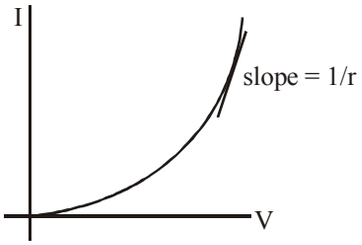
60. **(b,d)** We know that $\alpha = \frac{I_c}{I_e}$ and $\beta = \frac{I_c}{I_b}$

Also $I_e = I_b + I_c$

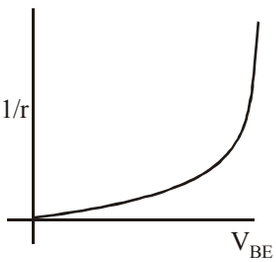
$\therefore \alpha = \frac{Ic}{I_b + I_c} = \frac{\frac{I_c}{I_b}}{1+\frac{I_c}{I_b}} = \frac{\beta}{1+\beta}$

Option (b) and (d) are therefore incorrect.

61. **(c)**



$\Rightarrow$

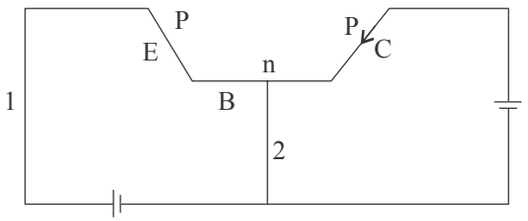


62. **(c)** For C.B. configuration $\frac{r_i}{r_o} \cong 0.1\Omega$

For CE and CC-configuration

$\frac{r_i}{r_0} \approx 1\Omega$.

63. **(c)** Connecting circuit according to question, it is clear



+ve terminal 1, –ve terminal 2, resistance high.

64. **(c)** In the given question, A, B and C refer base, collector and emitter respectively.

65. **(b)** It is a *p-n-p* transistor with *R* as base.

66. **(a)** Collector current, $I_C = 5.488$ mA,

Emitter current $I_e = 5.6$ mA

$\alpha = \frac{I_c}{I_e} = \frac{5.488}{5.6}$,

$\beta = \frac{\alpha}{1-\alpha} = 49$

67. **(d)** In common base amplifier circuit, input and output voltage are in the same phase. So, the phase difference between input voltage signal and output voltage signal is zero.

68. **(c)** In npn transistor, electrons moves from emitter to base.

69. **(d)** In common emitter configuration for transistor amplifier current gain

$A_i = \frac{-h_{fe}}{1+b_{oe}R_L}$

Where h_{fe} and h_{oe} are hybrid parameters.

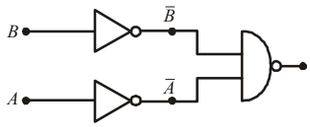
$\therefore A_i = \frac{-50}{1+25\times10^{-6}\times1\times10^{3}}$

$= -48.78$

70. **(a)** Emitter main function is to supply the majority charge carrriers towards the collector. Therefore emitter is most heavily doped.

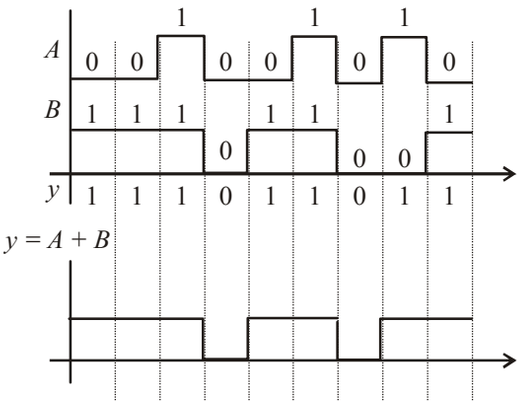
71. **(a)** Boolean expression,

$y = \overline{\bar{A}\cdot\bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A + B$



Truth table :

A	B	Y
0	1	1
1	0	1
0	0	0
1	1	1



72. **(c)** When two inputs of NAND gate is shorted, it behaves like a NOT gate so boolen equation will be

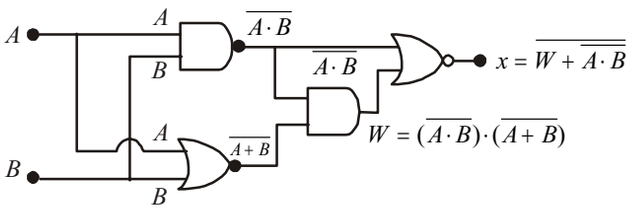
$y = \overline{\overline{A} + \overline{B} + \overline{C}}$

$y = A \cdot B \cdot C$

A	B	C	
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	1

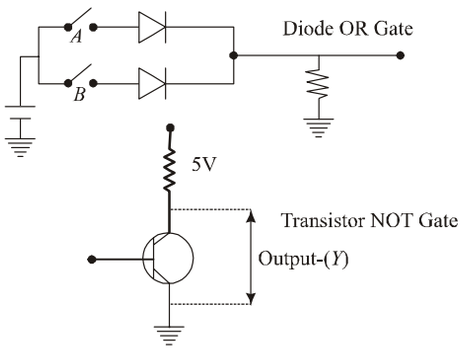
Thus, whole arrangement behaves like a AND gate.

73. **(a)**



A	B	$\overline{A \cdot B}$	$\overline{A+B}$	$W = (\overline{A \cdot B}) \cdot (\overline{A+B})$	$Q = W + \overline{A \cdot B}$	$\overline{Q} = x$
1	0	1	0	0	1	0
0	1	1	0	0	1	0
1	1	0	0	0	0	1
0	0	1	1	1	0	0

74. **(d)**

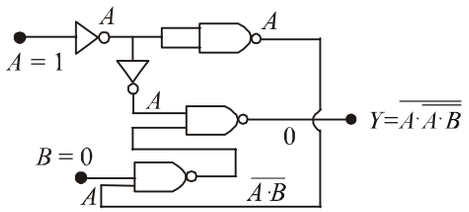


OR + NOT → NOR Gate

Hence Boolean relation at the output stage – Y for the circuit,

$Y = \overline{A+B} = \overline{A}.\overline{B}$

75. **(a)**



$Y = \overline{\overline{AB}.A} = \overline{\overline{AB}} + \overline{A} = AB + \overline{A}$

For $A = 1, B = 0$

$Y = (1) \times 0 + 0$

$\Rightarrow Y = 0 + 0 = 0$

76. **(d)** A logic gate is reversible if we can recover input data from the output. Hence NOT gate.

77. **(c)**

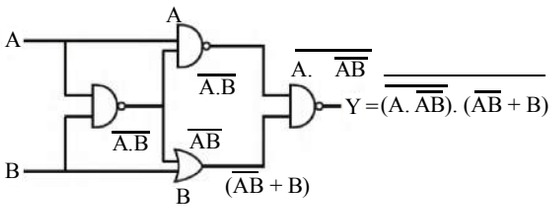
A	B	(A + B)	(A + B). A	$\overline{(A+B).A}$
0	0	0	0	1
0	1	1	0	1
1	0	1	1	0
1	1	1	1	0

78. **(b)** Truth table →

The output is of OR-gate

A	B	$\overline{A}$	$\overline{B}$	$\overline{\overline{A}.\overline{B}}$
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

79. **(c)**



$$Y=\left(\overline{A\cdot\overline{AB}}\right)+\left(\overline{\overline{AB}+B}\right)$$

$$=A\cdot\overline{AB}+AB\cdot\overline{B}$$

$$=A\cdot\left(\overline{A}+\overline{B}\right)+AB\cdot\overline{B}$$

$$=A\overline{B}$$

80. **(c)** From the given logic circuit,

$p=\overline{x}+y$

$Q=\overline{\overline{y}.x}=y+\overline{x}$

Output, $R=\overline{P+Q}$

To make output 1

P + Q must be '0'

So, x = 1, y = 0

81. **(c)** Truth table of the circuit is as follows

x	y	$\overline{x}$	$a=x.y$	$b=\overline{x}.y$	$z=\overline{a.b}$
0	0	1	0	0	1
0	1	1	0	1	1
1	0	0	0	0	1
1	1	0	1	0	1

82. **(a)** In case of an 'OR' gate the input is zero when all inputs are zero. If any one input is ' 1', then the output is '1'.

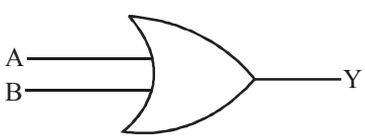
83. **(c)** Truth table for given logical circuit

a	b	(a + b)	c	Y = (a + b) .c
0	0	0	0	0
0	1	1	1	1
1	0	1	1	1
1	1	1	0	0

Output of OR gate must be 1 and c = 1

So, a = 1, b = 0 or a = 0, b = 1.

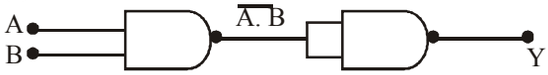
84. **(a)** It represents OR-Gate.



A	B	A + B = Y
0	0	0
0	1	1
1	0	1
1	1	1

85. **(a)** AND Gate

86. **(a)**



$$Y=\overline{\overline{AB}.\overline{AB}}=\overline{\overline{AB}}+\overline{\overline{AB}}=AB+AB=AB$$

In this case output Y is equivalent to AND gate.

87. **(a)** For circuit 1

$$A\,.\,B=\overline{Y+\overline{A}}=C$$

A	B		$\overline{Y+\overline{A}}$	= C
0	0	0	1	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

88. **(a)** In the given system all four gate is NOR gate

Truth Table

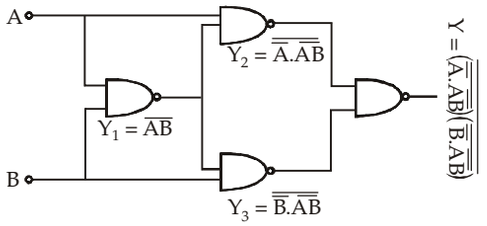
A	B	$(y'=\overline{A+B})$	$y''=(\overline{A+y'})$	$y'''=(A+y'')$	$y=\overline{y''+y'''}$
0	0	1	0	0	1
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

i.e.,

A	B	y
0	0	1
0	1	0
1	0	0
1	1	1

89. **(a)** The output at C corresponds to A NAND B or $\overline{A\cdot B}=C$

90. **(a)**



By expanding this Boolen expression

$Y=A.\overline{B}+B.\overline{A}$

Thus the truth table for this expression should be (a).

91. **(c)** Truth table is as shown :

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}+\overline{B}$	$\overline{\overline{A}+\overline{B}}$
0	0	1	1	1	0
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	0	1

Thus the combination of two NOT gates and one NOR gate is equivalent to a AND gate.

92. **(a)** NOR gate is the combination of NOT and OR gate.

Boolean expression for NOR gate is

$Y = \overline{A + B}$

93. **(b)** When either of A or B is 1 i.e. closed then lamp will glow.

In this case, Truth table

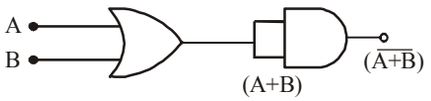
Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

This represents OR gate.

94. **(b)** When both inputs of NAND gate are jointed to form a single input, it behaves as NOT gate

OR + NOT = NOR.

$\left(\overline{A + B}\right)$ = NOR gate



95. **(a)** The final boolean expression of these gates is,

$X = \left(\overline{\bar{A}.\bar{B}}\right) = \bar{\bar{A}} + \bar{\bar{B}} = A + B \Rightarrow$ OR gate

It means OR gate is formed.

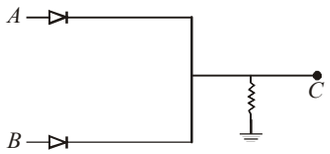
96. **(d)** The final boolean expression

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

$Y = (\overline{\bar{A} + \bar{B}}) = \bar{\bar{A}}.\bar{\bar{B}} = A \cdot B$.

Thus, it is an AND gate for which truth table is

97. **(d)**



The truth table for the above circuit is :

A	B	C
1	1	1
1	0	1
0	1	1
0	0	0

when either A or B conducts, the gate conducts. It means $C = A + B$ which is for OR gate.